

## WHAT IS CLAIMED IS:

- 1           1.    A method, comprising:
  - 2           identifying a setting for a capacitor bank associated with a
  - 3   voltage-controlled oscillator in a closed-loop phase-locked-loop,
  - 4   the setting representing a combination of one or more capacitors
  - 5   in the capacitor bank;
  - 6           estimating a gain introduced by the closed-loop phase-
  - 7   locked-loop when the oscillator operates using the identified
  - 8   setting;
  - 9           estimating a response of a loop filter in the phase-locked-
  - 10   loop;
  - 11          identifying one or more coefficients for a digital filter
  - 12   using the identified gain and the identified loop filter
  - 13   response, the digital filter operable to filter an input signal;
  - 14   and
  - 15          modulating the filtered input signal using the phase-locked-
  - 16   loop to produce an output signal.

1           2.    The method of Claim 1, wherein identifying the setting  
2   for the capacitor bank comprises:  
3           scaling the output signal produced by the voltage-controlled  
4   oscillator;  
5           clocking a counter using the scaled output signal to produce  
6   a counter signal;  
7           estimating a frequency of the counter signal a plurality of  
8   times;  
9           identifying differences between the estimated frequencies  
10   and a desired frequency;  
11          accumulating the differences;  
12          filtering the accumulated differences; and  
13          processing the filtered accumulated differences to produce  
14   the setting for the capacitor bank.

1           3.    The method of Claim 1, wherein estimating the gain  
2 introduced by the closed-loop phase-locked-loop comprises:

3           setting a desired frequency associated with the phase-  
4 locked-loop to a first value;

5           identifying a first input value to a digital-to-analog  
6 converter in a charge pump in the phase-locked-loop;

7           setting the desired frequency to a second value;

8           identifying a second input value to the digital-to-analog  
9 converter;

10          identifying a difference between the first and second input  
11 values; and

12          identifying the gain of the phase-locked-loop using the  
13 identified difference.

1           4.    The method of Claim 3, wherein the identified gain  
2 comprises an estimated unity gain bandwidth; and

3           further comprising:

4           identifying an ideal input value for the digital-to-  
5 analog converter;

6           rounding down the ideal input value to generate an  
7 actual input value; and

8           identifying an actual gain introduced by the phase-  
9 locked-loop using the actual input value.

1           5.    The method of Claim 4, wherein estimating the response  
2 of the loop filter comprises:

3           identifying an error between the ideal input value for the  
4 digital-to-analog converter and the actual input value; and

5           estimating the response of the loop filter using the  
6 identified error.

1           6.    The method of Claim 1, wherein identifying the one or  
2 more coefficients for the digital filter comprises:

3           identifying a transfer function from the input signal to the  
4 output signal;

5           transforming the transfer function to generate a transformed  
6 transfer function; and

7           calculating one or more values for the one or more  
8 coefficients using the transformed transfer function.

1           7.    The method of Claim 1, wherein the digital filter  
2 alters the input signal to at least partially compensate for an  
3 irregularity introduced into the output signal by the closed-loop  
4 phase-locked-loop.

1           8.    The method of Claim 1, wherein:  
2           the phase-locked-loop and the digital filter form at least a  
3   portion of a frequency synthesizer;  
4           the frequency synthesizer occupies no more than 4 mm<sup>2</sup> of  
5   space;  
6           the frequency synthesizer operates using no more than 35 mA  
7   of current; and  
8           the estimating steps, the identifying steps, and a time  
9   needed for the phase-locked-loop to settle collectively take no  
10   more than 140  $\mu$ s.

1           9.    A frequency synthesizer, comprising:  
2           a digital filter operable to receive and filter an input  
3    signal;  
4           a closed-loop phase-locked-loop comprising a voltage-  
5    controlled oscillator and a loop filter, the phase-locked-loop  
6    operable to receive the filtered input signal and generate an  
7    output signal; and  
8           a controller operable to:  
9                identify a setting for a capacitor bank associated with  
10    the voltage-controlled oscillator, the setting representing a  
11    combination of one or more capacitors in the capacitor bank;  
12                estimate a gain introduced by the phase-locked-loop  
13    when the oscillator operates using the identified setting;  
14                estimate a response of the loop filter;  
15                identify one or more coefficients for the digital  
16    filter using the identified gain and the identified loop filter  
17    response.

1        10. The frequency synthesizer of Claim 9, wherein the  
2 controller is operable to identify the setting for the capacitor  
3 bank by receiving the setting from a capacitor select circuit,  
4 the capacitor select circuit comprising:

5        a prescaler operable to scale the output signal produced by  
6 the voltage-controlled oscillator;

7        a counter operable to be clocked by the scaled output signal  
8 to produce a counter signal;

9        a digital frequency discriminator operable to estimate a  
10 frequency of the counter signal a plurality of times;

11       an adder operable to identify differences between the  
12 estimated frequencies and a desired frequency;

13       an integrator operable to accumulate the differences;

14       a low-pass filter operable to filter the accumulated  
15 differences; and

16       an averaging unit operable to average the filtered  
17 accumulated differences to produce the setting for the capacitor  
18 bank.

1        11. The frequency synthesizer of Claim 9, wherein the  
2 controller is operable to estimate the gain by:

3        setting a desired frequency associated with the phase-  
4 locked-loop to a first value;

5        identifying a first input value to a digital-to-analog  
6 converter in a charge pump in the phase-locked-loop;

7        setting the desired frequency to a second value;

8        identifying a second input value to the digital-to-analog  
9 converter;

10       identifying a difference between the first and second input  
11 values; and

12       identifying the gain of the phase-locked-loop using the  
13 identified difference.

1       12. The frequency synthesizer of Claim 11, wherein:

2       the identified gain comprises an estimated unity gain  
3 bandwidth; and

4       the controller is further operable to estimate the gain by:

5       identifying an ideal input value for the digital-to-  
6 analog converter;

7       rounding down the ideal input value to generate an  
8 actual input value; and

9       identifying an actual gain of the phase-locked-loop  
10 using the actual input value.



1        13. The frequency synthesizer of Claim 12, wherein the  
2 controller is operable to estimate the response of the loop  
3 filter by:

4        identifying an error between the ideal input value for the  
5 digital-to-analog converter and the actual input value; and

6        estimating the response of the loop filter using the  
7 identified error.

1        14. The frequency synthesizer of Claim 9, wherein the  
2 controller is operable to identify the one or more coefficients  
3 for the digital filter by:

4        identifying a transfer function from the input signal to the  
5 output signal;

6        transforming the transfer function to generate a transformed  
7 transfer function; and

8        calculating one or more values for the one or more  
9 coefficients using the transformed transfer function.

1        15. The frequency synthesizer of Claim 9, wherein the  
2 digital filter alters the input signal to at least partially  
3 compensate for an irregularity introduced into the output signal  
4 by the closed-loop phase-locked-loop.

1        16. The frequency synthesizer of Claim 9, wherein:  
2        the frequency synthesizer occupies no more than 4 mm<sup>2</sup> of  
3        space;  
4        the frequency synthesizer operates using no more than 35 mA  
5        of current; and  
6        the frequency synthesizer is operable to perform the  
7        estimating and the identifying functions and the phase-locked-  
8        loop is operable to settle collectively within no more than 140  
9         $\mu$ s.

1        17. A wireless device, comprising:  
2        an antenna operable to transmit outgoing signals over a  
3        wireless interface; and  
4        a transceiver operable to generate the outgoing signals, the  
5        transceiver comprising a frequency synthesizer, the frequency  
6        synthesizer comprising:  
7            a digital filter operable to receive and filter an  
8        input signal;  
9            a closed-loop phase-locked-loop comprising a voltage-  
10       controlled oscillator and a loop filter, the phase-locked-loop  
11       operable to receive the filtered input signal and generate the  
12       outgoing signal; and  
13       a controller operable to:  
14            identify a setting for a capacitor bank associated  
15       with the voltage-controlled oscillator, the setting representing  
16       a combination of one or more capacitors in the capacitor bank;  
17            estimate a gain introduced by the phase-locked-  
18       loop when the oscillator operates using the identified setting;  
19            estimate a response of the loop filter; and  
20            identify one or more coefficients for the digital  
21       filter using the identified gain and the identified loop filter  
22       response.

1        18. The wireless device of Claim 17, wherein the controller  
2        is operable to identify the setting for the capacitor bank by  
3        receiving the setting from a capacitor select circuit, the  
4        capacitor select circuit comprising:

5        a prescaler operable to scale the outgoing signal produced  
6        by the voltage-controlled oscillator;

7        a counter operable to be clocked by the scaled outgoing  
8        signal to produce a counter signal;

9        a digital frequency discriminator operable to estimate a  
10       frequency of the counter signal a plurality of times;

11       an adder operable to identify differences between the  
12       estimated frequencies and a desired frequency;

13       an integrator operable to accumulate the differences;

14       a low-pass filter operable to filter the accumulated  
15       differences; and

16       an averaging unit operable to average the filtered  
17       accumulated differences to produce the setting for the capacitor  
18       bank.

1        19. The wireless device of Claim 17, wherein the controller  
2        is operable to estimate the gain and the response by:

3        setting a desired frequency associated with the phase-  
4        locked-loop to a first value;

5        identifying a first input value to a digital-to-analog  
6        converter in a charge pump in the phase-locked-loop;

7        setting the desired frequency to a second value;

8        identifying a second input value to the digital-to-analog  
9        converter;

10       identifying a difference between the first and second input  
11       values;

12       estimating a unity gain bandwidth of the phase-locked-loop  
13       using the identified difference;

14       identifying an ideal input value for the digital-to-analog  
15       converter;

16       rounding down the ideal input value to generate an actual  
17       input value;

18       identifying an actual gain of the phase-locked-loop using  
19       the actual input value;

20       identifying an error between the ideal input value for the  
21       digital-to-analog converter and the actual input value; and

22       estimating the response of the loop filter using the  
23       identified error..

1        20. The wireless device of Claim 17, wherein the controller  
2        is operable to identify the one or more coefficients for the  
3        digital filter by:  
4        identifying a transfer function from the input signal to the  
5        outgoing signal;  
6        transforming the transfer function to generate a transformed  
7        transfer function; and  
8        calculating one or more values for the one or more  
9        coefficients using the transformed transfer function.